

Electrical Solution to Enable High-Speed Memory Interfaces

ABSTRACT

According to one embodiment of the present invention, a circuit is disclosed. The circuit includes: a plurality of memory modules; a memory controller coupled to the plurality of memory modules; a plurality of bus splitters coupled between the plurality of memory modules and the memory controller to split signals communicated between the plurality of memory modules and the memory controller; and a plurality of terminators to reduce signal reflections corresponding to the split signals.